



**PRODUCT NAME :** CD4046 Micropower Phase-locked Loop

**PRICE :** Rs 29.00

**SKU :** RM0701



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## DESCRIPTION

## Features

- Consisting of a Linear, Voltage-Controlled Oscillator and two Phase Comparators
- The VCO Produces an Output Signal Whose Frequency is Determined by the Input Voltage
- Inhibit Control Pin
- Operating Temperature to 85oC
- Low Power TTL



October 1987  
 Revised January 1999

## CD4046BC Micropower Phase-Locked Loop

### General Description

The CD4046BC micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO<sub>IN</sub> input, and the capacitor and resistors connected to pin C1<sub>A</sub>, C1<sub>B</sub>, R1 and R2.

The source follower output of the VCO<sub>IN</sub> (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

### Features

- Wide supply voltage range: 3.0V to 18V
- Low dynamic power consumption: 70 μW (typ.) at f<sub>o</sub> = 10 kHz, V<sub>DD</sub> = 5V
- VCO frequency: 1.3 MHz (typ.) at V<sub>DD</sub> = 10V
- Low frequency drift: 0.06%/°C at V<sub>DD</sub> = 10V with temperature
- High VCO linearity: 1% (typ.)

### Applications

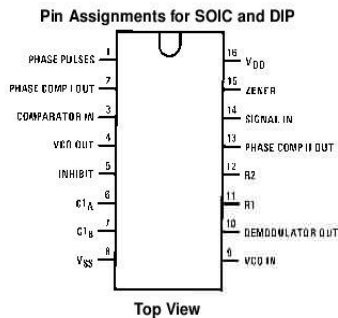
- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

### Ordering Code:

Order Number	Package Number	Package Description
CD4046BCM	M16A	16-Lead Small Outline integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD4046BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



**Absolute Maximum Ratings** (Note 1)

(Note 2)

DC Supply Voltage ( $V_{DD}$ )	-0.5 to +18 $V_{DC}$
Input Voltage ( $V_{IN}$ )	-0.5 to $V_{DD}$ +0.5 $V_{DC}$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 2)

DC Supply Voltage ( $V_{DD}$ )	3 to 15 $V_{DC}$
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$ $V_{DC}$
Operating Temperature Range ( $T_A$ )	-40°C to +85°C

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	Pin 5 = $V_{DD}$ , Pin 14 = $V_{DD}$ , Pin 3, 9 = $V_{SS}$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		20		0.005	20		150	$\mu A$
				40		0.01	40		300	$\mu A$
				80		0.015	80		600	$\mu A$
		Pin 5 = $V_{DD}$ , Pin 14 = Open, Pin 3, 9 = $V_{SS}$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		70		5	55		205	$\mu A$
	530			20	410		710	$\mu A$		
	1500			50	1200		1800	$\mu A$		
$V_{OL}$	LOW Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
$V_{OH}$	HIGH Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
$V_{IL}$	LOW Level Input Voltage Comparator and Signal In	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or 9V		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0		6.25	4.0		4.0	V
$V_{IH}$	HIGH Level Input Voltage Comparator and Signal In	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0	8.25		11.0		V
$I_{OL}$	LOW Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
$I_{OH}$	HIGH Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.44	-0.88		-0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
$I_{IN}$	Input Current	All Inputs Except Signal Input $V_{DD} = 15V, V_{IN} = 0V$		-0.3		-10 <sup>-5</sup>	-0.3		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10 <sup>-5</sup>	0.3		1.0	$\mu A$
$C_{IN}$	Input Capacitance	Any Input (Note 3)					7.5			pF
$P_T$	Total Power Dissipation	$f_o = 10$ kHz, $R1 = 1$ M $\Omega$ , $R2 = \infty, \zeta X O_{IN} = \zeta_{MAX} / 2$ $V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$				0.07				mW
						0.6				mW
						2.4				mW

**Note 3:** Capacitance is guaranteed by periodic testing.

**Note 4:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

